RomWBW

Hardware

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Chapter 1

Overview

1.1 Supported Platforms

This section contains a summary of the system configuration target for each of the pre-built ROM images included in the RomWBW distribution.

It is intended to help you select the correct ROM image and understand the basic hardware components supported. Detailed hardware system configuration information should be obtained from your system provider/designer.

The table below summarizes the hardware platforms currently supported by RomWBW along with the standard pre-built ROM image(s).

RCBUS - General Configurations

RCBus refers to Spencer Owen's RC2014 bus specification and derivatives including RC26, RC40, RC80, and BP80.

Description	Bus	ROM Image File	Baud Rate
RCBus Z80 CPU Module, 512K RAM/ROM	RCBus	RCZ80_std.rom	115200
RCBus Z80 CPU Module (KIO), 512K w/KIO	RCBus	RCZ80_kio_std.rom	115200
RCBus Z180 CPU Module (External)	RCBus	RCZ180_ext_std.rom	115200
RCBus Z180 CPU Module (Native)	RCBus	RCZ180_nat_std.rom	115200
RCBus Z280 CPU Module (External)	RCBus	RCZ280_ext_std.rom	115200
RCBus Z280 CPU Module (Native)	RCBus	RCZ280_nat_std.rom	115200

KIO refers to a Zilog specific Serial/Parallel Counter/Timer (Z84C90).

The RCBus Z180 & Z280 require a separate RAM/ROM memory module. There are two types of these modules, you must pick the correct ROM for your type of memory module:

- The first type of RAM/ROM module includes Z2 style memory bank switching on the memory module itself. This is called "External" (ext) because the bank switching is external from the CPU itself.
- The second type of RAM/ROM module has no bank switching logic on the memory module. Bank switching is implemented via the Z180 or Z280 MMU – this is called "Native" (nat) because the CPU itself provides the bank switching logic.

Only Z180 and Z280 CPUs have the ability to do bank switching in the CPU, so the ext/nat selection only applies to them. Z80 CPUs have no built-in bank switching logic, so they always require a RAM/ROM module with Z2 style bank switching and the ROMs are always configured for external bank switching.

Custom / Specific Configurations

Andrew Lynch

Description	Bus	ROM Image File	Baud Rate
RetroBrew Z80 SBC V2	ECB	SBC_std.rom	38400
RetroBrew Z80 SimH	-	SBC_simh.rom	38400
Duodyne Z80 System	Duo	DUO_std.rom	38400
Nhyodyne Z80 MBC	MBC	MBC_std.rom	38400
Rhyophyre Z180 SBC	-	RPH_std.rom	38400
N8 Z180 SBC (date >= 2312)	ECB	N8_std.rom	38400

Bill Shen

Description	Bus	ROM Image File	Baud Rate
EaZy80-512 Z80 CPU Module	RCBus	RCZ80_ez512_std.rom	115200
K80W Z80 CPU Module	RCBus	RCZ80_k80w_std.rom	115200
ZRC Z80 CPU Module	RCBus	RCZ80_zrc_std.rom	115200
ZRC Z80 CPU Module (RAM)	RCBus	RCZ80_zrc_ram_std.rom	115200
ZRC512 Z80 CPU Module	RCBus	RCZ80_zrc512_std.rom	115200
Z1RCC Z180 CPU Module	RCBus	RCZ180_z1rcc_std.rom	115200
ZZRCC Z280 CPU Module	RCBus	RCZ280_zzrcc_std.rom	115200
ZZRCC Z280 CPU Module (RAM)	RCBus	RCZ280_zzrcc_ram_std.rom	115200
ZZ80MB Z280 SBC	RCBus	RCZ280_zz80mb_std.rom	115200

Sergey Kiselev

Description	Bus	ROM Image File	Baud Rate
Easy Z80 SBC	RCBus	EZZ80_easy_std.rom	115200
Tiny Z80 SBC	RCBus	EZZ80_tiny_std.rom	115200
Z80-512K CPU/RAM/ROM Module	RCBus	RCZ80_skz_std.rom	115200
Zeta Z80 SBC , ParPortProp	-	ZETA_std.rom	38400
Zeta V2 Z80 SBC , ParPortProp	-	ZETA2_std.rom	38400

Stephen Cousins

Description	Bus	ROM Image File	Baud Rate
SC126 Z180 SBC	BP80	SCZ180_sc126_std.rom	115200
SC130 Z180 SBC	RCBus	SCZ180_sc130_std.rom	115200
SC131 Z180 Pocket Comp	-	SCZ180_sc131_std.rom	115200
SC140 Z180 CPU Module	Z50	SCZ180_sc140_std.rom	115200
SC503 Z180 CPU Module	Z50	SCZ180_sc503_std.rom	115200
SC700 Z180 CPU Module	RCBus	SCZ180_sc700_std.rom	115200

Others

Description	Bus	ROM Image File	Baud Rate
Dyno Z180 SBC[2]	Dyno	DYNO_std.rom	38400
EP Mini-ITX Z180[6]	UEXT	EPITX_std.rom	115200
eZ80 for RCBus Module[8], 512K RAM/ROM	RCBus	RCEZ80_std.rom	115200
Genesis Z180 System[7]	STD	GMZ180_std.rom	115200
Heath H8 Z80 System[5]	H8	HEATH_std.rom	115200
MSX[9]	MSX	MSX_std.rom	115200
N8 PC[10]	ISA	N8PC_std.rom	38400
NABU w/ RomWBW Option Board[5]	NABU	NABU_std.rom	115200
S100 Computers Z180 SBC[4]	S100	SZ180_std.rom	57600
S100 Computers Z80 CPU[4]	S100	SZ80_std.rom	19200
S100 Computers T35 FPGA Z80 SBC[4]	S100	SZ80_t35.rom	9600
UNA Hardware BIOS[1]	-	UNA_std.rom	-
Z80-Retro SBC[3]	-	Z80RETRO_std.rom	38400
Z180 Mark IV SBC[1]	ECB	MK4_std.rom	38400

[1] Designed by John Coffman
[2] Designed by Steve Garcia
[3] Designed by Peter Wilson
[4] Designed by John Monahan
[5] Designed by Les Bird
[6] Designed by Alan Cox
[7] Designed by Doug Jackson
[8] Designed by Dean Netherton
[9] MSX Port by Henk Berends
[10] Designed by Dan Werner

1.2 General Guidance

The standard ROM images will detect and install support for certain devices and peripherals that are on-board or frequently used with each platform. If the device or peripheral is not detected at boot, the ROM will simply bypass support appropriately.

Each ROM will support a single memory manager. This is determined by the build configuration and is not dynamically selected. The use of the term Memory Manager is generally synonymous with Memory Management Unit (MMU).

In some cases, support for multiple hardware components with potentially conflicting resource usage are handled by a single ROM image. It is up to the user to ensure that no conflicting hardware is in use.

CPU speed will be dynamically measured at startup if DSRTC is present

All pre-built ROM images are pure binary files (they are not “hex” files). They are intended to be programmed starting at the very start of the ROM chip (address 0). Most of the pre-built images are 512KB in size. If your system utilizes a larger ROM, you can just program the image into the first 512KB of the ROM for now.

For this document port addresses `IO=xxx` are represented in decimal.

The PropIO support is based on RomWBW specific firmware. Be sure to program/update your PropIO firmware with the corresponding firmware image provided in the Binary directory of the RomWBW distribution.

The use of high density floppy disks requires a CPU speed of 8 MHz or greater.

Chapter 2

Platform Configurations

2.1 Duodyne Z80 System

Duodyne is a third generation ROMWBW focused retrocomputer incorporating lessons learned and improvements from my original ECB Z80 SBC (aka N8VEM) and the nhyodyne modular computer. It is literally designed around ROMWBW from the start for a robust OS and software environment.

Duodyne is a new design which integrates many functions into larger, modular boards on a backplane. The intent is to create a powerful and capable system like an SBC, but with modularity and an expandable backplane.

- Creator: Andrew Lynch
- Retrobrew Forums: Introducing duodyne retrocomputer
- Github: DuoDyne

ROM Image File: DUO_std.rom

Bus	Duo
Default CPU Speed	8.000 MHz
Interrupts	Mode 2
System Timer	CTC
Serial Default	38400 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=66, SWIO=66
- DSRTC: MODE=STD, IO=148
- PCF: IO=86
- UART: IO=88
- UART: IO=168
- UART: IO=112
- UART: IO=120
- SIO MODE=ZP, IO=96, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=ZP, IO=96, CHANNEL B, INTERRUPTS ENABLED
- LPT: MODE=SPP, IO=72
- DMA: MODE=DUO, IO=64
- CH: IO=78
- CHUSB: IO=78
- CHSD: IO=78
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=DUO, IO=128, DRIVE 0, TYPE=3.5” HD
- FD: MODE=DUO, IO=128, DRIVE 1, TYPE=3.5” HD
- PPIDE: IO=136, MASTER
- PPIDE: IO=136, SLAVE
- SD: MODE=MT, IO=140, UNITS=1
- SPK: IO=148
- CTC: IO=96, TIMER MODE=COUNTER, DIVISOR=18432, HI=256, LO=72, INTERRUPTS ENABLED

2.2 Dyno Z180 SBC

The Dyno Computer is a Zilog Z180-based computer initially designed to run Wayne Warthen's ROMWBW

- Creator: Steve García
- Google Groups: An Introduction
- Website: Dyno Computer

ROM Image File: DYNO_std.rom

Bus	Dyno•Bus
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	38400 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- BQRTC: IO=80
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=DYNO, IO=132, DRIVE 0, TYPE=3.5" HD
- FD: MODE=DYNO, IO=132, DRIVE 1, TYPE=3.5" HD
- PPIDE: IO=76, MASTER
- PPIDE: IO=76, SLAVE

2.3 EP Mini-ITX Z180

EtchedPixels Z180 Mini-ITX. The SC126 was almost my ideal retrobrew Z80/Z180 system but with a couple of niggles and lack of a convenient case option. This is the same core Z180 CPU/RAM/ROM design taken the other direction, of expandability.

- Creator: Alan Cox
- Google Groups: Another new board
- Github: Z180MiniITX

ROM Image File: EPITX_std.rom

Bus	RCBus + UEXT
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=160
- UART: IO=168
- TMS: MODE=MSX, IO=152, SCREEN=40X24, KEYBOARD=NONE
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=EPFDC, IO=72, DRIVE 0, TYPE=3.5” HD
- FD: MODE=EPFDC, IO=72, DRIVE 1, TYPE=3.5” HD
- SD: MODE=EPITX, IO=66, UNITS=1

2.4 Easy/Tiny Z80

2.4.1 Easy Z80 SBC

This project is a simple, easy to understand, yet capable single board computer. It reuses the same memory paging mechanism I've implemented in Zeta SBC V2. It uses Zilog Z80 SIO/O and Z80 CTC peripheral ICs and implements daisy chain mode 2 interrupt configuration

(Not to be confused with EaZy80)

- Creator: Sergey Kiselev
- Google Groups: Easy Z80 - Single Board Computer
- Github: Easy_Z80

ROM Image File: EZZ80_easy_std.rom

Bus	RCBus
Default CPU Speed	10.000 MHz
Interrupts	Mode 2
System Timer	CTC
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- INTRTC: ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=STD, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=STD, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60

- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1
- CTC: IO=136, TIMER MODE=COUNTER, DIVISOR=18432, HI=256, LO=72, INTERRUPTS ENABLED

2.4.2 Tiny Z80 SBC

Tiny Z80 is a business card sized (size?!) single board computer (SBC). It is mostly compatible with Easy Z80, and offers similar capabilities Tiny Z80 includes a USB to Serial converter IC on board connected to one of the SIO ports, for ease of use with modern computers.

- Creator: Sergey Kiselev
- Github: Tiny_Z80

ROM Image File: EZZ80_tiny_std.rom

Bus	RCBus
Default CPU Speed	16.000 MHz
Interrupts	Mode 2
System Timer	CTC
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- INTRTC: ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=STD, IO=24, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=STD, IO=24, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM

- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=144, MASTER
- IDE: MODE=RC, IO=144, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1
- CTC: IO=16, TIMER MODE=COUNTER, DIVISOR=18432, HI=256, LO=72, INTERRUPTS ENABLED

2.5 S100 Computers

2.5.1 S100 Computers Z80 CPU

Z80-based S100 Modular System

- Creator: John Monahan
- Website: S100 Computers Z80 CPU

ROM Image File: SZ80_std.rom

Bus	S100
Default CPU Speed	8.000 MHz
Interrupts	None
System Timer	None
Serial Default	19200 Baud
Memory Manager	SZ80
ROM Size	0 KB
RAM Size	1024 KB

Supported Hardware

- FP: LEDIO=5
- PLDSER: IO=172
- SCC MODE=SZ80, IO=160, CHANNEL A
- SCC MODE=SZ80, IO=160, CHANNEL B
- SCON: IO=0
- ESPSD: IO=128, PRIMARY
- ESPSD: IO=128, SECONDARY
- MD: TYPE=RAM
- PPIDE: MODE=S100A, IO=48, MASTER
- PPIDE: MODE=S100A, IO=48, SLAVE
- PPIDE: MODE=S100B, IO=48, MASTER
- PPIDE: MODE=S100B, IO=48, SLAVE

Notes:

- Initial console will depend on the IOBYTE dip switch settings. See website for dip switch settings.

- Version 6.0 or greater of the S100 Z80 Monitor ROM is required to load and run RomWBW.
- RomWBW is loaded by the S100 monitor from either CF Card or SD Card. The CF/SD Card should be imaged using SZ80_std_hd1k_combo.img which includes RomWBW.

2.5.2 S100 Computers T35 FPGA Z80 SBC

A T35 FPGA Z80 based S100 SBC

- Creator: John Monahan
- Website: S100 Computers FPGA Z80 SBC

ROM Image File: SZ80_t35.rom

Bus	S100
Default CPU Speed	8.000 MHz
Interrupts	None
System Timer	None
Serial Default	19200 Baud
Memory Manager	Z2
ROM Size	0 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=255
- DS5RTC: RTCIO=104, IO=104
- TSER: IO=53
- PLDSER: IO=172
- SCC MODE=SZ80, IO=160, CHANNEL A
- SCC MODE=SZ80, IO=160, CHANNEL B
- LPT: MODE=T35, IO=199
- TVGA: IO=192, KBD MODE=T35, KBD IO=3
- KBD: ENABLED
- SCON: IO=0
- ESPSD: IO=128, PRIMARY
- ESPSD: IO=128, SECONDARY
- MD: TYPE=RAM
- PPIDE: MODE=STD, IO=48, MASTER
- PPIDE: MODE=STD, IO=48, SLAVE
- PPIDE: MODE=S100A, IO=56, MASTER
- PPIDE: MODE=S100A, IO=56, SLAVE
- PPIDE: MODE=S100B, IO=56, MASTER
- PPIDE: MODE=S100B, IO=56, SLAVE
- SD: MODE=T35, IO=108, UNITS=2

Notes:

- This RomWBW build is specifically for the Trion T35 based module on the S100 Z80 FPGA board. The Waveshare FPGA module is not supported at this time.
- Requires matching FPGA code, see S100 Projects RomWBW T35 Project.
- Initial console will depend on the IOBYTE dip switch settings. See website for dip switch settings.
- RomWBW is loaded by the S100 monitor from either CF Card or SD Card. The CF/SD Card should be imaged using SZ80_t35_hd1k_combo.img which includes RomWBW.

2.6 Genesis Z180 System

A Z180 based board with 512k ram, 512k rom, dual serial / parallel, RTC and SD Card, based on the STD bus. This was inspired on Pulsar Little Big board and some designs of Stephen Cousins

- Creator: Doug Jackson
- Specific Links not Available

ROM Image File: GMZ180_std.rom

Bus	STD
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- GM7303: IO=48
- DSRTC: MODE=STD, IO=132
- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- IDE: MODE=GIDE, IO=32, MASTER
- IDE: MODE=GIDE, IO=32, SLAVE
- SD: MODE=GM, IO=132, UNITS=1

2.7 Heath H8 Z80 System

Turn your H8 into a RomWBW CP/M computer

- Creator: Les Bird
- Github Wiki: H8-Z80-ROMWBW-V1.0

ROM Image File: HEATH_std.rom

Bus	H8
Default CPU Speed	16.384 MHz
Interrupts	Mode 1
System Timer	None
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- H8P: IO=240
- INTRTC: ENABLED
- UART: IO=232
- UART: IO=224
- UART: IO=216
- UART: IO=208
- TMS: MODE=MSX, IO=152, SCREEN=80X24, KEYBOARD=NONE
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- AY38910: MODE=MSX, IO=160, CLOCK=1789772 HZ

2.8 Z180 Mark IV SBC

The Z180 Mark IV is a single board computer, meaning it may run stand-alone. It also has an interface to the RetroBrew bus (ECB) for access to additional peripheral boards.

- Creator: John Coffman
- Retrobrew Wiki: Z180 Mark IV

ROM Image File: MK4_std.rom

Bus	ECB
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	38400 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- DSRTC: MODE=STD, IO=138
- ASCI: IO=64, INTERRUPTS ENABLED
- ASCI: IO=65, INTERRUPTS ENABLED
- UART: IO=24
- UART: IO=128
- UART: IO=192
- UART: IO=200
- UART: IO=208
- UART: IO=216
- VGA: IO=224, KBD MODE=PS/2, KBD IO=224
- CVDU: MODE=ECB, IO=224, KBD MODE=PS/2, KBD IO=226
- KBD: ENABLED
- PRP: IO=168
- PRPCON: ENABLED
- PRPSD: ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=DIDE, IO=42, DRIVE 0, TYPE=3.5” HD
- FD: MODE=DIDE, IO=42, DRIVE 1, TYPE=3.5” HD

- IDE: MODE=MK4, IO=128, MASTER
- IDE: MODE=MK4, IO=128, SLAVE
- SD: MODE=MK4, IO=137, UNITS=1

2.9 MSX

Support for standard MSX hardware by Henk Berends

The default configuration is for a European MSX 2 (PAL) with international keyboard and 512KB RAM Mapper extension.

ROM Image File: MSX_std.rom

Bus	MSX
Default CPU Speed	3.579 MHz
Interrupts	Mode 1
System Timer	TMS
Serial Default	115200 Baud
Memory Manager	MSX
ROM Size	0 KB
RAM Size	448 KB

Supported Hardware

- RP5C01: IO=180
- UART: IO=128
- UART: IO=136
- TMS: MODE=MSXMKY, IO=152, SCREEN=80X24, KEYBOARD=MKY, INTERRUPTS ENABLED
- MKY: IO=168
- MD: TYPE=RAM
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: MODE=MSX_BEER, IO=48, MASTER
- PPIDE: MODE=MSX_BEER, NO SLAVE
- AY38910: MODE=MSX, IO=160, CLOCK=1789772 HZ

Notes:

- MSX 1 can be used with the TMS VDP set to 40 columns mode.
- Storage options are the BEER IDE and SODA IDE interfaces.
- Serial option is a 16550 UART interface.

2.10 NABU w/ RomWBW Option Board

No modifications to the NABU motherboard needed. Leave the standard NABU ROM in its socket on the motherboard, no need to remove it. You can switch back to standard NABU mode by changing one jumper on the Option Card

- Creator: Les Bird
- Github Wiki: NABU RomWBW Option Card

ROM Image File: NABU_std.rom

Bus	NABU
Default CPU Speed	3.580 MHz
Interrupts	Mode 2
System Timer	TMS
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- NABU: IO=64
- INTRTC: ENABLED
- UART: IO=72
- TMS: MODE=NABU, IO=160, SCREEN=80X24, KEYBOARD=NABU, INTERRUPTS ENABLED
- NABUKB: IO=144
- MD: TYPE=RAM
- MD: TYPE=ROM
- PPIDE: IO=96, MASTER
- PPIDE: IO=96, SLAVE
- AY38910: MODE=NABU, IO=65, CLOCK=1789772 HZ

Notes:

- TMS video assumes F18A replacement for TMS9918

2.11 Nhyodyne Z80 MBC

Nhyodyne: A Modular Backplane Computer (MBC).

The purpose of this project is to revisit the design concepts behind my original Z80 SBC (aka test prototype) which has evolved into the SBC V2-005 over several years. Attempt to introduce some new concepts to make the design more modular, flexible, and less expensive.

The MBC consists of four core boards: Z80 backplane, Z80 processor, Z80 clock, and Z80 ROM. These are sufficient to build a working system of minimum capability.

- Creator: Andrew Lynch
- Retrobrew Forums: Z80 Multi Board Computer
- Github: NhyoDyne
- Retrobrew Wiki: Z80 Modular Backplane Computer

ROM Image File: MBC_std.rom

Bus	MBC
Default CPU Speed	8.000 MHz
Interrupts	None
System Timer	None
Serial Default	38400 Baud
Memory Manager	MBC
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- PKD: IO=96, SIZE=8X1
- DSRTC: MODE=STD, IO=112
- UART: IO=104
- UART: IO=128
- UART: IO=136
- SIO MODE=ZP, IO=176, CHANNEL A
- SIO MODE=ZP, IO=176, CHANNEL B
- PIO: IO=184, CHANNEL A
- PIO: IO=184, CHANNEL B
- PIO: IO=188, CHANNEL A
- PIO: IO=188, CHANNEL B
- LPT: MODE=SPP, IO=232

- CVDU: MODE=MBC, IO=224, KBD MODE=PS/2, KBD IO=226
- TMS: MODE=MBC, IO=152, SCREEN=80X24, KEYBOARD=KBD
- KBD: ENABLED
- ESP: IO=156
- ESPCON: ENABLED
- ESPSER: DEVICE=0
- ESPSER: DEVICE=1
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=MBC, IO=48, DRIVE 0, TYPE=3.5” HD
- FD: MODE=MBC, IO=48, DRIVE 1, TYPE=3.5” HD
- PPIDE: IO=96, MASTER
- PPIDE: IO=96, SLAVE
- SPK: IO=112

2.12 RetroBrew Z80

2.12.1 RetroBrew Z80 SBC V2

The SBC V2 is a Zilog Z80 processor board. It's a 100x160mm board that is capable of functioning both as a standalone SBC or as attached to the ECB bus.

Previously known as the N8VEM SBC, after Andrews Ham radio call sign, development began in 2006 wth V1 and is currently still in development, it launched a tsunami of developments based on the Euro Card Bus (ECB) standard.

- Creator: Andrew Lynch
- Github: SBC-V2-005 (May not be official)
- Github: SBC-V2-004
- Retrobrew Wiki: SBC V2
- Blog: Building the SBCV2 Z80

ROM Image File: SBC_std.rom

Bus	ECB
Default CPU Speed	8.000 MHz
Interrupts	None
System Timer	None
Serial Default	38400 Baud
Memory Manager	SBC
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- DSRTC: MODE=STD, IO=112
- UART: MODE=SBC, IO=104
- UART: MODE=CAS, IO=128
- UART: MODE=MFP, IO=104
- UART: MODE=4UART, IO=192
- UART: MODE=4UART, IO=200
- UART: MODE=4UART, IO=208
- UART: MODE=4UART, IO=216
- VGA: IO=224, KBD MODE=PS/2, KBD IO=224
- CVDU: MODE=ECB, IO=224, KBD MODE=PS/2, KBD IO=226
- CVDU occupies 905 bytes.

- KBD: ENABLED
- PRP: IO=168
- PRPCON: ENABLED
- PRPSD: ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=DIO, IO=54, DRIVE 0, TYPE=3.5” HD
- FD: MODE=DIO, IO=54, DRIVE 1, TYPE=3.5” HD
- PPIDE: IO=96, MASTER
- PPIDE: IO=96, SLAVE

2.12.2 RetroBrew Z80 SimH

Image for Altair Z80 SimH emulator

ROM Image File: SBC_simh.rom

Bus	-
Default CPU Speed	8.000 MHz
Interrupts	Mode 1
System Timer	SimH
Serial Default	38400 Baud
Memory Manager	SBC
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- SIMRTC: IO=254
- SSER: IO=109
- MD: TYPE=RAM
- MD: TYPE=ROM
- HDSK: IO=253, DEVICE COUNT=2

Notes:

- CPU speed and Serial configuration not relevant in emulator

2.13 N8 Z180 SBC

The N8 is intended to be a “home brew” style computer in the style of early 1980’s all-in-one home computers with a usable set of features such as color graphics, audio, an assortment of mass storage options, a variety of ports, etc. Although a bus expansion is supported no additional boards are required.

This configuration is for the N8-2312 and latter (4314) revisions

- Creator: Andrew Lynch
- Retrobrew Wiki: The N8
- Blog: A Z180 based SBC

ROM Image File: N8_std.rom

Bus	ECB
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	38400 Baud
Memory Manager	N8
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- DSRTC: MODE=STD, IO=136
- ASCI: IO=64, INTERRUPTS ENABLED
- ASCI: IO=65, INTERRUPTS ENABLED
- TMS: MODE=N8, IO=152, SCREEN=40X24, KEYBOARD=PPK
- PPK: ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=N8, IO=140, DRIVE 0, TYPE=3.5” HD
- FD: MODE=N8, IO=140, DRIVE 1, TYPE=3.5” HD
- SD: MODE=CSIO, IO=136, UNITS=1
- AY38910: MODE=N8, IO=156, CLOCK=1789772 HZ

Notes:

- SD Card interface is configured for CSIO (N8 date code >= 2312)

2.14 N8 PC

This is a variant of the N8 computer.

- Creator: Dan Werner
- Project GitHub: N8 PC

ROM Image File: N8PC_std.rom

Bus	ISA
Default CPU Speed	9.216 MHz
Interrupts	None
System Timer	Z180
Serial Default	38400 Baud
Memory Manager	N8
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- PKD: IO=132, SIZE=8X1
- M6242RTC: IO=160
- ASCI: IO=64
- ASCI: IO=65
- TMS: MODE=N8PC, IO=152, SCREEN=80X24, KEYBOARD=KBD
- KBD: ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=N8, IO=140, DRIVE 0, TYPE=3.5” HD
- FD: MODE=N8, IO=140, DRIVE 1, TYPE=3.5” HD
- PPIDE: MODE=STD, IO=132, MASTER
- PPIDE: MODE=STD, IO=132, SLAVE
- AY38910: MODE=N8, IO=156, CLOCK=3579545 HZ

Notes:

2.15 RCBus Z80

2.15.1 RCBus Z80 CPU Module

Generic Rom Image.

ROM Image File: RCZ80_std.rom

Bus	RCBus
Default CPU Speed	7.372 MHz
Interrupts	Mode 1
System Timer	None
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- ACIA: IO=128, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER

- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.15.2 RCBus Z80 CPU Module (KIO)

Generic Rom Image. SIO Serial baud rate managed by CTC

ROM Image File: RCZ80_kio_std.rom

Bus	RCBus
Default CPU Speed	7.372 MHz
Interrupts	Mode 2
System Timer	CTC
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- INTRTC: ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=STD, IO=136, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=STD, IO=136, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

- KIO: IO=128
- CTC: IO=132, TIMER MODE=TIMER/16, DIVISOR=9216, HI=256, LO=36, INTERRUPTS ENABLED

2.15.3 Z80-512K CPU/RAM/ROM Module

Z80-512K is an RCBus and RC2014* compatible module, designed to run RomWBW firmware including CP/M, ZSDOS, and various applications under these OSes. Z80-512K combines functionality of CPU, RAM, and ROM on a single module, thus saving space on the backplane.

- Creator: Sergey Kiselev
- Google Groups: Z80-512K
- Github: Z80-512K

ROM Image File: RCZ80_skz_std.rom

Bus	RCBus
Default CPU Speed	7.372 MHz
Interrupts	Mode 1
System Timer	None
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- ACIA: IO=128, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM

- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.15.4 ZRC Z80 CPU Module

ZRC is derived from the ZoRC experiment. The basic notion is that large RAM and fast serial upload enable a diskless CP/M SBC. However, just in case that idea didn't work out, ZRC has an optional compact flash interface. The targeted software for ZRC is ROMWBW. ZRC physically contains no ROM and 2MB of RAM.

In the STD configuration the first 512KB of RAM is loaded with a ROM image from disk storage and then handled like ROM. Essentially, an area of the RAM is reserved to act as ROM.

- Creator: Bill Shen
- Retrobrew Wiki: ZRC, Z80 RAM CPLD for ROMWBW
- Google Groups: ZRC, Z80/RAM/CPLD, minimal CP/M-ready, Z80 SBC

ROM Image File: RCZ80_zrc_std.rom

Bus	RCBus
Default CPU Speed	14.745 MHz
Interrupts	Mode 1
System Timer	None
Serial Default	115200 Baud
Memory Manager	ZRC
ROM Size	512 KB
RAM Size	1536 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- ACIA: IO=128, INTERRUPTS ENABLED
- VRC: IO=0, KBD MODE=VRC, KBD IO=244
- KBD: ENABLED

- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.15.5 ZRC Z80 CPU Module (RAM)

This profile differs (from STD) only in how the system boots, and how RAM is configured. Boot occurs directly to RAM, loading HBIOS directly from disk storage rather than via a pseudo ROM image copied into RAM.

A RAM disk is configured preloaded with files that would normally be on the ROM disk. There is no ROM disk in this configuration.

The RAM config is the newer approach and provides a more efficient bank layout. The intent to replace the STD config with the RAM config.

- Creator: Bill Shen

ROM Image File: RCZ80_zrc_ram_std.rom

Bus	RCBus
Default CPU Speed	14.745 MHz
Interrupts	Mode 1
System Timer	None
Serial Default	115200 Baud
Memory Manager	ZRC
ROM Size	0 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- ACIA: IO=128, INTERRUPTS ENABLED
- VRC: IO=0, KBD MODE=VRC, KBD IO=244
- KBD: ENABLED

- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.15.6 ZRC512 Z80 CPU Module

ZRC512 is a faster and hobbyist-friendly variant of ZRC. It is designed specifically for ROM-less RomWBW. HBIOS is loaded from disk at boot

- Creator: Bill Shen
- Google Groups: Bill Shen's ZRC512 SBC / RC2014 board
- Retrobrew Wiki: ZRC512, A Hobbyist-friendly Z80 SBC for ROM-less RomWBW

ROM Image File: RCZ80_zrc512_std.rom

Bus	RCBus
Default CPU Speed	22.000 MHz
Interrupts	Mode 1
System Timer	None
Serial Default	115200 Baud
Memory Manager	ZRC
ROM Size	0 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- ACIA: IO=128, INTERRUPTS ENABLED
- VRC: IO=0, KBD MODE=VRC, KBD IO=244
- KBD: ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60

- MD: TYPE=RAM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.15.7 EaZy80-512 Z80 CPU Module

Eazy80-512 is Eazy80 rev2 pc board configured with 512K RAM to run RomWBW. The design was derived from modifications to Eazy80 Rev1 that supported RomWBW.

HBIOS is loaded from disk at boot by ROM monitor or via a a compressed ROM image.

(Not to be confused with EasyZ80)

- Creator: Bill Shen
- VCF Forums: Eazy80, a glue-less, CP/M capable Z80 SBC
- Retrobrew Wiki: Eazy80 Rev2, Glue-less Configuration
- Google Groups: EaZy80, A Simple80 with KIO

ROM Image File: RCZ80_ez512_std.rom

Bus	RCBus
Default CPU Speed	22.000 MHz
Interrupts	Mode 2
System Timer	None
Serial Default	115200 Baud
Memory Manager	EZ512
ROM Size	0 KB
RAM Size	512 KB

Compressed ROM Image File: RCZ80_ez512_std_64k.rom

The RomWBW utility program ‘compress’ is designed to squeeze the compiled RomWBW 128K file ‘RCZ80_ez512_std.upd’ into a 64K ROM. As there are many areas in RomWBW with repeating bytes of the same value, it is possible to compress the 128K file to fit into a 64K ROM.

The compression program looks for two or more consecutive bytes of the same value (any values of $00 to $FF). If it finds duplicates, it leaves two of the duplicate bytes followed by a byte count, n-1 (n <= $FF), where n is the total number of duplicates. If the program succeeds in compressing the input file to fit into the available space, the file ‘RCZ80_ez512_std_64k.rom’ is constructed, along with a short Z80 decompression program that will be stored in the last 256 bytes of the ROM. The constructed 64K file is saved and the unused storage space is output in bytes. Should compression fail to fit the input file into available space, only an error message and the overrun in bytes is output.

The decompression program, located at $FF00, is executed at startup via the 3-byte jump at

location $0000, decompressing the stored code in ROM into the computer's RAM. When decompression finishes, control is passed to RAM location $0000, which in turn starts execution of RomWBW.

The 64K ROM Layout:

- The first 3 bytes are always $C3 $00 $FF, a jump to the Z80 decompression code located at $FF00 in the ROM.
- Locations $0003 up to, and including, $FEFF are available to store the compressed 128K input file.
- Location $FF00 up to, and including, $FFFF, is where the Z80 decompression program is stored.

Supported Hardware

- DSRTC: MODE=STD, IO=192
- SIO MODE=STD, IO=8, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=STD, IO=8, CHANNEL B, INTERRUPTS ENABLED
- MD: TYPE=RAM
- MD occupies 409 bytes.
- SD: MODE=EZ512, IO=2, UNITS=1
- KIO: IO=0
- CTC: IO=4

2.15.8 K80W Z80 CPU Module

K80W is similar to K80. It is a 22MHz Z80 SBC with KIO (Z84C90) as the I/O device. It is designed to run RomWBW. The current version is rev 2.1 replacing the older K80W rev 1

- Creator: Bill Shen
- Retrobrew Wiki: K80W Rev2.1, A RomWBW-capable Z80 SBC

ROM Image File: RCZ80_k80w_std.rom

Bus	RCBus
Default CPU Speed	22.000 MHz
Interrupts	Mode 2
System Timer	None
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=K80W, IO=192
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=STD, IO=136, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=STD, IO=136, CHANNEL B, INTERRUPTS ENABLED
- VRC: IO=0, KBD MODE=VRC, KBD IO=244
- KBD: ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD

- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=EZ512, IO=130, UNITS=1
- KIO: IO=128
- CTC: IO=132

2.16 RCBus Z180

2.16.1 RCBus Z180 CPU Module (External)

Generic Rom Image. For use with Z2 bank switched memory board (Z2 external memory management)

ROM Image File: RCZ180_ext_std.rom

Bus	RCBus
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- DSRTC: MODE=STD, IO=12
- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD

- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.16.2 RCBus Z180 CPU Module (Native)

Generic Rom Image. For use with linear memory board (Z180 native memory management)

ROM Image File: RCZ180_nat_std.rom

Bus	RCBus
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- DSRTC: MODE=STD, IO=12
- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE

- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.16.3 Z1RCC Z180 CPU Module

Z1RCC is a 2“x4” RomWBW-capable Z180 SBC.

Z1RCC has no flash memory on board but has a small (64 bytes) bootstrap ROM in CPLD so that Z180 boots from this bootstrap ROM, copies a loader from CF disk to top 32K of RAM, runs the loader to bring in the 480K RomWBW image from CF disk, then start RomWBW from 0x0

- Creator: Bill Shen
- Google Groups: RomWBW for Z80 with 512K RAM 0K ROM
- Retrobrew Wiki: Z1RCC, A RC2014-Compatible, RomWBW-Capable Z180 SBC

ROM Image File: RCZ180_z1rcc_std.rom

Bus	RCBus
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	0 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- DSRTC: MODE=STD, IO=12
- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60

- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.17 RCBus Z280

2.17.1 RCBus Z280 CPU Module (External)

Generic Rom Image. For use with Z2 bank switched memory board (Z2 external memory management)

ROM Image File: RCZ280_ext_std.rom

Bus	RCBus
Default CPU Speed	12.000 MHz
Interrupts	Mode 1
System Timer	None
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- INTRTC: ENABLED
- Z2U: IO=16
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- ACIA: IO=128, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM

- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.17.2 RCBus Z280 CPU Module (Native)

Generic Rom Image. For use with linear memory board (Z280 native memory management)

ROM Image File: RCZ280_nat_std.rom

Bus	RCBus
Default CPU Speed	12.000 MHz
Interrupts	Mode 3
System Timer	Z280
Serial Default	115200 Baud
Memory Manager	Z280
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- INTRTC: ENABLED
- Z2U: IO=16, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE

- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=PIO, IO=105, UNITS=1

2.17.3 ZZRCC Z280 CPU Module

ZZRCC follows the basic concept of ZRCC that uses a small CPLD to bootstrap from CF disk. Because Z280 has a native serial-bootstrap capability, the CPLD is even simpler than that of ZRCC. ZZRCC is Z280 operating in Z80-compatible mode. It is designed for RC2014 bus ZZRCC actually contains no ROM and 512KB of RAM.

In the STD configuration the first 256KB of RAM is loaded with a ROM image from disk storage and then handled like ROM. Essentially, an area of the RAM is reserved to act as ROM.

- Creator: Bill Shen
- Retrobrew Wiki: ZZRCC, a SBC for RC2014 based on Z280
- Google Groups: ZZRCC, Z280 SBC replacing ZZ80RC and ZZ80CF
- Google Groups: Help porting ROMWBW to ZZRCC

ROM Image File: RCZ280_zzrcc_std.rom

Bus	RCBus
Default CPU Speed	14.745 MHz
Interrupts	Mode 3
System Timer	Z280
Serial Default	115200 Baud
Memory Manager	Z280
ROM Size	256 KB
RAM Size	256 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- INTRTC: ENABLED
- Z2U: IO=16, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED

- VRC: IO=0, KBD MODE=VRC, KBD IO=244
- KBD: ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE

2.17.4 ZZRCC Z280 CPU Module (RAM)

This profile differs (from STD) only in how the system boots, and how RAM is configured. Boot occurs directly to RAM, loading HBIOS directly from disk storage rather than via a pseudo ROM image copied into RAM.

A RAM disk is configured preloaded with files that would normally be on the ROM disk. There is no ROM disk in this configuration.

The RAM config is the newer approach and provides a more efficient bank layout. The intent to replace the STD config with the RAM config.

- Creator: Bill Shen

ROM Image File: RCZ280_zzrcc_ram_std.rom

Bus	RCBus
Default CPU Speed	14.745 MHz
Interrupts	Mode 3
System Timer	Z280
Serial Default	115200 Baud
Memory Manager	Z280
ROM Size	0 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- INTRTC: ENABLED
- Z2U: IO=16, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- VRC: IO=0, KBD MODE=VRC, KBD IO=244

- KBD: ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE

2.17.5 ZZ80MB Z280 SBC

ZZ80MB is a Z280-based motherboard with RC2014 expansion slots. It is based on the ZZ80RC-CF design, but with two additional expansion slots added. ZZ80MB is designed with an EPROM programmer function such that it can boot from serial port, load EPROM programming image through the serial port and program an EPROM. This feature can be used to program EPROM for other computers

- Creator: Bill Shen
- Retrobrew Wiki: ZZ80MB, A Z280-based SBC with RC2014 Expansion

ROM Image File: RCZ280_zz80mb_std.rom

Bus	RCBus
Default CPU Speed	12.000 MHz
Interrupts	Mode 3
System Timer	Z280
Serial Default	115200 Baud
Memory Manager	Z280
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- DSRTC: MODE=STD, IO=192
- INTRTC: ENABLED
- Z2U: IO=16, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- VRC: IO=0, KBD MODE=VRC, KBD IO=244
- KBD: ENABLED
- CH: IO=62

- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE

2.18 eZ80 for RCBus Module

The eZ80 for RCBus/RC2014 is a module designed for the RCBus and RC2014 backplanes.

Its designed as a 'compatible upgrade' to the stock Z80 CPU. The eZ80 is a CPU that was first released by Zilog about 20 years ago, and still available from the manufacturer today

- Creator: Dean Netherton
- Github: eZ80 for the RCBus/RC2014
- Hackaday: eZ80 CPU for RC2014 and other backplanes

ROM Image File: RCEZ80_std.rom

Bus	RCBus
Default CPU Speed	20.000 MHz
Interrupts	Mode 1
System Timer	EZ80
Serial Default	115200 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- LCD: IO=218, SIZE=20X4
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5" HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5" HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- EZ80: CPU DRIVER
- EZ80: SYS TIMER DRIVER
- EZ80: RTC DRIVER

- EZ80: UART DRIVER

2.19 Rhyophyre Z180 SBC

Single Board Computer featuring Zilog Z180 processor and NEC µPD7220 Graphics Display Controller

- Creator: Andrew Lynch
- Retrobrew Forums: Z180 upd7220 GDC SBC
- Github: rhyophyre

ROM Image File: RPH_std.rom

Bus	-
Default CPU Speed	18.432 MHz
Interrupts	None
System Timer	None
Serial Default	38400 Baud
Memory Manager	RPH
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- DSRTC: MODE=STD, IO=132
- ASCI: IO=64
- ASCI: IO=65
- GDC: MODE=RPH, DISPLAY=EGA, IO=144
- KBD: ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- PPIDE: IO=136, MASTER
- PPIDE: IO=136, SLAVE

2.20 S100 Computers Z180 SBC

A Z180 board which contains a flash RAM, a USB port interface and an SD Card that can immediately boot up CPM. While it is on an S100 Bus board, initially that board has only 8 significant chips and works as a self contained computer outside the bus with a simple 9V power supply.

Later on it can be built up further with more chips, placed in an S100 bus and one by one programed to interface with the 100's of S100 bus cards that are out there. It can in fact behave as a S100 bus master or slave as defined by the IEEE-696 specs.

- Creator: John Monahan |
- Website: S100 Computers Z180 SBC

ROM Image File: SZ180_std.rom

Bus	S100
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	57600 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- INTRTC: ENABLED
- PLDSER: IO=172
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- SCC MODE=SZ80, IO=160, CHANNEL A
- SCC MODE=SZ80, IO=160, CHANNEL B
- SCON: IO=0
- ESPSD: IO=128, PRIMARY
- ESPSD: IO=128, SECONDARY
- MD: TYPE=RAM
- MD: TYPE=ROM
- PPIDE: MODE=S100A, IO=48, MASTER
- PPIDE: MODE=S100A, IO=48, SLAVE
- PPIDE: MODE=S100B, IO=48, MASTER

- PPIDE: MODE=S100B, IO=48, SLAVE
- SD: MODE=SC, IO=12, UNITS=1

Notes:

- Z180 SBC SW2 (IOBYTE) Dip Switches:

Bit	Setting	Function
0	Off	Use Z180 ASCI Channel A for console
	On	Use Propeller Console
1	Off	Boot to RomWBW Boot Loader
	On	Boot to S100 Monitor

2.21 Small Computer Central Z180

Small Computer Central provides an extensive range hardware based around the Zilog ecosystem. This section lists configurations specifically for the Z180 processor

If you are using a Z80 processor you will probably be using the general `RCZ80_std` configuration - RCBus Z80 CPU Module. However, please consult Firmware, RomWBW, RCZ80_std for further information and to ensure compatibility with your Z80 system.

- Creator: Stephen Cousins
- Website: Small Computer Central

2.21.1 SC126 Z180 SBC

SC126 is a Z180 Motherboard.

- Website: SC126 – Z180 Motherboard

ROM Image File: SCZ180_sc126_std.rom

Bus	BP80
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=13, SWIO=0
- DSRTC: MODE=STD, IO=12
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED

- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=SC, IO=12, UNITS=1

Notes:

- When disabled, watchdog requires /IM to be pulsed. If an RCBus module holds the CPU in WAIT for more than this, the watchdog will fire when disabled with random consequences. The Pico SD does this at power-on.

2.21.2 SC130 Z180 SBC

SC130 is an entry-level Z180 Motherboard designed primarily to run RomWBW (and CP/M)

- Website: SC130 – Z180 Motherboard

ROM Image File: SCZ180_sc130_std.rom

Bus	RCBus
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0, SWIO=0
- DSRTC: MODE=STD, IO=12
- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD

- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=SC, IO=12, UNITS=1

2.21.3 SC131 Z180 Pocket Comp

SC131 is a pocket-sized Z180 RomWBW CP/M computer.

- Website: SC131 – Z180 Pocket Computer

ROM Image File: SCZ180_sc131_std.rom

Bus	-
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- SD: MODE=SC, IO=12, UNITS=1

2.21.4 SC140 Z180 CPU Module

SC140 is a Z180 SBC / Z50Bus Card card.

- Website: SC140 – Z180 SBC / Z50Bus Card

ROM Image File: SCZ180_sc140_std.rom

Bus	Z50
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=160, SWIO=160
- DSRTC: MODE=STD, IO=12
- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD

- IDE: MODE=RC, IO=144, MASTER
- IDE: MODE=RC, IO=144, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=SC, IO=12, UNITS=1

2.21.5 SC503 Z180 CPU Module

SC503 is a Z180 Processor card designed for Z50Bus.

- Website: SC503 – Z180 Processor (Z50Bus)

ROM Image File: SCZ180_sc503_std.rom

Bus	Z50
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=160, SWIO=160
- DSRTC: MODE=STD, IO=12
- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD

- IDE: MODE=RC, IO=144, MASTER
- IDE: MODE=RC, IO=144, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=SC, IO=12, UNITS=1

2.21.6 SC700 Z180 CPU Module

This configuration is specifically for systems based on the Z180 CPU (eg. SC722) with 1MB linear memory (eg. SC721)

- Website: SC700 Series
- Website: SC721 – RCBus Memory Module
- Website: SC722 – RCBus Z180 CPU Module

ROM Image File: SCZ180_sc700_std.rom

Bus	RCBus
Default CPU Speed	18.432 MHz
Interrupts	Mode 2
System Timer	Z180
Serial Default	115200 Baud
Memory Manager	Z180
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- FP: LEDIO=0
- LCD: IO=170, SIZE=20X4
- DSRTC: MODE=STD, IO=12
- INTRTC: ENABLED
- ASCI: IO=192, INTERRUPTS ENABLED
- ASCI: IO=193, INTERRUPTS ENABLED
- UART: IO=128
- UART: IO=136
- UART: IO=160
- UART: IO=168
- SIO MODE=RC, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=128, CHANNEL B, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=RC, IO=132, CHANNEL B, INTERRUPTS ENABLED
- CH: IO=62
- CH: IO=60
- CHUSB: IO=62
- CHUSB: IO=60

- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=RCWDC, IO=80, DRIVE 0, TYPE=3.5” HD
- FD: MODE=RCWDC, IO=80, DRIVE 1, TYPE=3.5” HD
- IDE: MODE=RC, IO=16, MASTER
- IDE: MODE=RC, IO=16, SLAVE
- PPIDE: IO=32, MASTER
- PPIDE: IO=32, SLAVE
- SD: MODE=SC, IO=12, UNITS=1

2.22 Z80-Retro SBC

The system comprises a Z80 retro computer board, and optonal VGA text video card, and PIO Keyboard and Sound Card. The system uses a custom 60 pin bus on a standard header.

(Not to be confused with a similar named project by John Winans presented by John's Basement on youTube)

- Creator: Peter Wilson
- Github: Z80-Retro
- Github Wiki: Welcome to the Z80-Retro wiki!
- OSHWLab: Simple Z80 SBC

ROM Image File: Z80RETRO_std.rom

Bus	60 pin
Default CPU Speed	14.745 MHz
Interrupts	Mode 2
System Timer	None
Serial Default	38400 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- SIO MODE=Z80R, IO=128, CHANNEL A, INTERRUPTS ENABLED
- SIO MODE=Z80R, IO=128, CHANNEL B, INTERRUPTS ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- SD: MODE=Z80R, IO=104, UNITS=1

2.23 Zeta Z80 SBC

Zeta SBC is an Zilog Z80 based single board computer. It is inspired by Ampro Little Board Z80 and N8VEM project. Zeta SBC is software compatible with N8VEM SBC and Disk I/O boards.

- Creator: Sergey Kiselev
- Retrobrew Wiki: Zeta SBC

ROM Image File: ZETA_std.rom

Bus	-
Default CPU Speed	8.000 MHz
Interrupts	None
System Timer	None
Serial Default	38400 Baud
Memory Manager	SBC
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- DSRTC: MODE=STD, IO=112
- UART: IO=104
- PPP: IO=96
- PPPCON: ENABLED
- PPPSD: ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=DIO, IO=54, DRIVE 0, TYPE=3.5” HD

Notes:

- If ParPortProp is installed, initial console output is determined by JP1:
  - Shorted: console to on-board serial port
  - Open: console to ParPortProp video and keyboard

2.24 Zeta V2 Z80 SBC

Zeta SBC V2 is a redesigned version of Zeta SBC.

Compared to the first version this version features updated MMU with four banks, each one of those banks can be mapped to any 16 KiB page in 1 MiB on-board memory. It adds Z80 CTC which is used for generating periodic interrupts and as a vectored interrupt controller for UART and PPI. The FDC is replaced with 37C65. Compared to FDC9266 used in Zeta SBC it integrates input/output buffers and floppy disk control latch. Additionally 37C65 FDC is easier to obtain than FDC9266. And lastly it is made using CMOS technology and more power efficient than FDC9266

- Creator: Sergey Kiselev
- Github: Zeta SBC V2
- Retrobrew Wiki: Zeta SBC V2

ROM Image File: ZETA2_std.rom

Bus	-
Default CPU Speed	8.000 MHz
Interrupts	Mode 2
System Timer	CTC
Serial Default	38400 Baud
Memory Manager	Z2
ROM Size	512 KB
RAM Size	512 KB

Supported Hardware

- DSRTC: MODE=STD, IO=112
- UART: IO=104
- PPP: IO=96
- PPPCON: ENABLED
- PPPSD: ENABLED
- MD: TYPE=RAM
- MD: TYPE=ROM
- FD: MODE=ZETA2, IO=48, DRIVE 0, TYPE=3.5” HD
- CTC: IO=32, TIMER MODE=COUNTER, DIVISOR=18432, HI=256, LO=72, INTERRUPTS ENABLED

Notes:

- If ParPortProp is installed, initial console output is determined by JP1:
  - Shorted: console to on-board serial port
  - Open: console to ParPortProp video and keyboard

Chapter 3

Device Drivers

This section briefly describes each of the possible devices that may be discovered by RomWBW in your system.

3.1 Character

ID	Description
ACIA	MC68B50 Asynchronous Communications Interface Adapter
ASCI	Zilog Z180 CPU Built-in Serial Ports
DUART	SCC2681 or compatible Dual UART
ESPCON	ESP32 Firmware-based Video Console
ESPSER	ESP32 Firmware-based Serial Interface
EZ80UART	eZ80 Serial Interface
LPT	Parallel I/O Controller
PIO	Zilog Parallel Interface Controller
PPPCON	ParPortProp Serial Console Interface
PRPCON	PropIO Serial Console Interface
SCON	S100 Console
SIO	Zilog Serial Input/Output Controller (SIO)
SCC	Zilog Serial Communications Controller (SCC)
SSER	Simple Serial Interface
TSER	Trion FPGA Serial Interface
PLDSER	PLD USB Serial Interface
UART	16C550 Family Serial Interface
USB-FIFO	FT232H-based ECB USB FIFO

ID	Description
Z2U	Zilog Z280 CPU Built-in Serial Ports

By default, RomWBW will use the first available character device it discovers for the initial console. The following character devices are scanned in the order shown. The available character devices depend on the active platform and configuration.

1. ASCI: Zilog Z180 CPU Built-in Serial Ports
2. Z2U: Zilog Z280 CPU Built-in Serial Ports
3. UART: 16C550 Family Serial Interface
4. DUART: SCC2681 or compatible Dual UART
5. SIO: Zilog Serial Port Interface (SIO)
6. SCC: Zilog Serial Port Interface (SCC)
7. EZ80UART: eZ80 Serial Port Interface
8. ACIA: MC68B50 Asynchronous Communications Interface Adapter
9. SSER: Simple Serial Interface
10. TSER: Trion FPGA Serial Interface
11. PLDSER: PLD USB Serial Interface
12. USB-FIFO: FT232H-based ECB USB FIFO

3.2 Disk

ID	Description
CHSD	CH37x SD Card Interface
CHUSB	CH37x USB Drive Interface
FD	Intel 8272 or compatible Floppy Disk Controller
HDSK	SIMH Simulator Hard Disk
IDE	IDE/ATA/ATAPI Hard Disk Interface
IMM	Zip Drive on PPI (IMM variant)
MD	ROM/RAM Disk
PPA	Zip Drive on PPI (PPA variant)
PPIDE	8255 IDE/ATA/ATAPI Hard Disk Interface
PPPSD	ParPortProp SD Card Interface
PRPSD	PropIO SD Card Interface
RF	RAM Floppy Disk Interface
SD	SD Card Interface
SYQ	Iomega SparQ Drive on PPI

ID	Description
ESPSD	S100 ESP32-based SD Card Interface

3.3 Video

ID	Description
CVDU	MC8563-based Video Display Controller
EF	EF9345 Video Display Controller
TVGA	S100 Trion FPGA Onboard VGA/Keyboard
GDC	uPD7220 Video Display Controller
TMS	TMS9918/38/58 Video Display Controller
VDU	MC6845 Family Video Display Controller (*)
VGA	HD6445CP4-based Video Display Controller
VRC	VGARC Video Display Controller
XOSERA	XOSERA FPGA-based Video Display Controller

Note:

- Reading bytes from the video memory of the VDU board (not Color VDU) appears to be problematic. This is only an issue when the driver needs to scroll a portion of the screen which is done by applications such as WordStar or ZDE. You are likely to see screen corruption in this case.

3.4 Keyboard

ID	Description
KBD	8242 PS/2 Keyboard Controller
MSXKYB	MSX Compliant Matrix Keyboard
NABUKB	NABU Keyboard
PPK	Matrix Keyboard

3.5 Audio

ID	Description
AY	AY-3-8910/YM2149 Programmable Sound Generator
SN76489	SN76489 Programmable Sound Generator
SPK	Bit-bang Speaker
YM	YM2612 Programmable Sound Generator

3.6 RTC (RealTime Clock)

ID	Description
BQRTC	BQ4845P Real Time Clock
DS5RTC	Maxim DS1305 SPI Real-Time Clock w/ NVRAM
DS7RTC	Maxim DS1307 PCF I2C Real-Time Clock w/ NVRAM
DS1501RTC	Maxim DS1501/DS1511 Watchdog Real-Time Clock
DSRTC	Maxim DS1302 Real-Time Clock w/ NVRAM
EZ80RTC	eZ80 Real-Time Clock
INTRTC	Interrupt-based Real Time Clock
PCRTC	MC146818/DS1285/DS12885 PC style
PCF	PCF8584-based I2C Real-Time Clock
RP5C01	Ricoh RPC01A Real-Time Clock w/ NVRAM
SIMRTC	SIMH Simulator Real-Time Clock
MMRTC	NS MM58167B Real-Time Clock (no NVRAM)
DS12RTC	Dallas Semiconductor DS1288x Real-Time Clock w/ NVRAM
M6242	MSM6242 Real-Time Clock (no NVRAM)

3.7 DsKy (DiSplay KeYpad)

ID	Description
FP	Simple LED & Switch Front Panel
GM7303	Prolog 7303 derived Display/Keypad
H8P	Heath H8 Display/Keypad
ICM	ICM7218-based Display/Keypad on PPI
LCD	Hitachi HD44780-based LCD Display
PKD	P8279-based Display/Keypad on PPI

3.8 System

ID	Description
CH	CH375/376 USB Interface Controller
CTC	Zilog Clock/Timer
DMA	Zilog DMA Controller
ESP	ESP32 Firmware-based interface
EZ80TIMER	eZ80 System Timer
KIO	Zilog Serial/ Parallel Counter/Timer (Z84C90)
PPP	ParPortProp Host Interface Controller
PRP	PropIO Host Interface Controller

Chapter 4

UNA Hardware BIOS

John Coffman has produced a new generation of hardware BIOS called UNA. The standard RomWBW distribution includes its own hardware BIOS. However, RomWBW can alternatively be constructed with UNA as the hardware BIOS portion of the ROM. If you wish to use the UNA variant of RomWBW, then just program your ROM with the ROM image called “UNA_std.rom” in the Binary directory. This one image is suitable on **all** of the platforms and hardware UNA supports.

UNA is customized dynamically using a ROM based setup routine and the setup is persisted in the system NVRAM of the RTC chip. This means that the single UNA-based ROM image can be used on most of the RetroBrew platforms and is easily customized. UNA also supports FAT file system access that can be used for in-situ ROM programming and loading system images.

While John is likely to enhance UNA over time, there are currently a few things that UNA does not support:

- Floppy Drives
- Terminal Emulation
- Zeta 1, N8, RCBus, Easy Z80, and Dyno Systems
- Some older support boards

The UNA version embedded in RomWBW is the latest production release of UNA. RomWBW will be updated with John’s upcoming UNA release with support for VGA3 as soon as it reaches production status.

Please refer to the UNA BIOS Firmware Page for more information on UNA.

4.1 UNA Usage Notes

- At startup, UNA will display a prompt similar to this:

  ```
  Boot UNA unit number or ROM? [R,X,0..3] (R):
  ```

  You generally want to choose 'R' which will then launch the RomWBW loader. Attempting to boot from a disk using a number at the UNA prompt will only work for the legacy (hd512) disk format. However, if you go to the RomWBW loader, you will be able to perform a disk boot on either disk format.

- The disk images created and distributed with RomWBW do not have the correct system track code for UNA. In order to boot to disk under UNA, you must first use `SYSCOPY` to update the system track of the target disk. The UNA ROM disk has the correct system track files for UNA: `CPM.SYS` and `ZSYS.SYS`. So, you can boot a ROM OS and then use one of these files to update the system track.

- The only operating systems supported at this time are CP/M 2 and ZSDOS. NZ-COM is also supported because it uses the ZSDOS CBIOS. None of the other RomWBW operating systems are supported such as CP/M 3, ZPM3, and p-System.

- Some of the RomWBW-specific applications are not UNA compatible.